Solutions for PTP wireless transmission
and networking applications

Technical Paper

2 Wire Voice Networking using the Aprisa XE

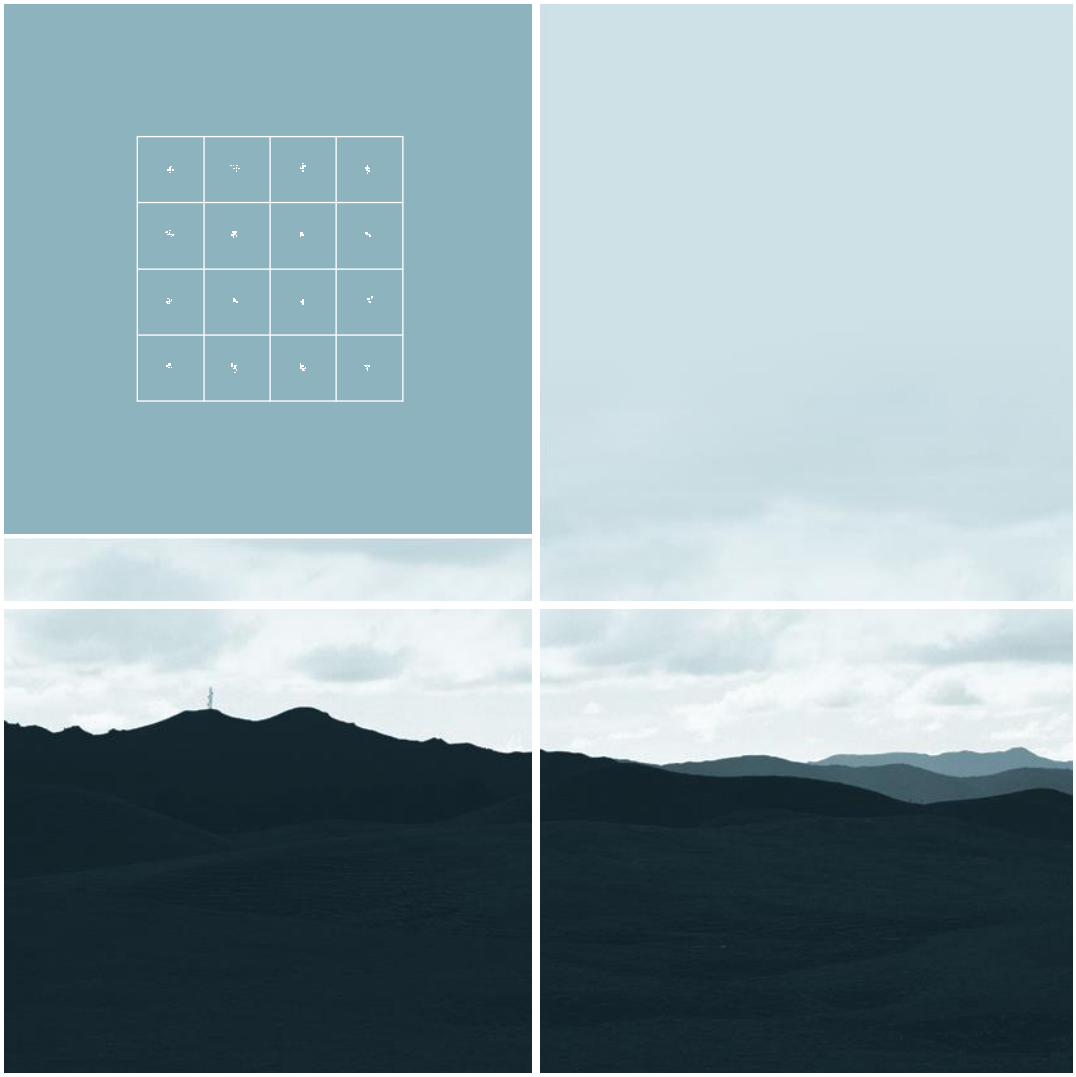


Table of Contents

The 2 Wire Loop Interface

Introduction

This technical note looks at the history, engineering and performance of 2 wire voice circuits using the Aprisa XE.

History

The 2 wire loop interface, often called POTS (Plain Old Telephone Service) was originally devised many years ago mainly to halve the number of cable pairs required to interconnect between telephones. This was in the days before any form of electronics where all communication, local and national, was by cable pair and all switching was done with operators using manual boards.

Automatic exchanges replaced manual boards and electronic transmission systems replaced the long haul copper but due to the proliferation of 2 wire loop telephones, the 2 wire loop interface remained.

Derived Systems, Circuits and the Aprisa XE

Derived Systems

Originally, telephone exchanges were located to service all the customers in a radius of about 12 km which is the maximum operating range of a typical exchange line card over a 0.4mm copper pair.

With the advent of electronic systems, derived systems were created that could extend the range that a telephone exchange could service.

Foreign Exchange Circuits

Circuits provisioned with derived systems were call Foreign Exchange circuits hence the terms;

- FXO Foreign Exchange Office
- FXS Foreign Exchange Subscriber

The purpose of derived loop interface circuits FXO / FXS is to transparently extend the 2 wire interface from the exchange line card to the telephone / PBX ideally without loss or distortion.

The Aprisa XE uses the generic terms of FXO / FXS and adds the D for dual interface.

The DFXO interface simulates the function of a telephone and a DFXS interface simulates the function of an exchange line card.

These circuits are known as ‘ring out, dial in’ 2 wire loop circuits.

Aprisa XE

Derived systems multiplex multiple loop interfaces via a TDM backplane into a high bitrate digital signal which is then transported over the digital bearer system e.g. copper bearer, radio bearer or fibre optic bearer.

The digital multiplex and the transport system are often separate products, but the Aprisa XE integrates both the digital multiplex and transport into one product.

E1 Frame and Signalling

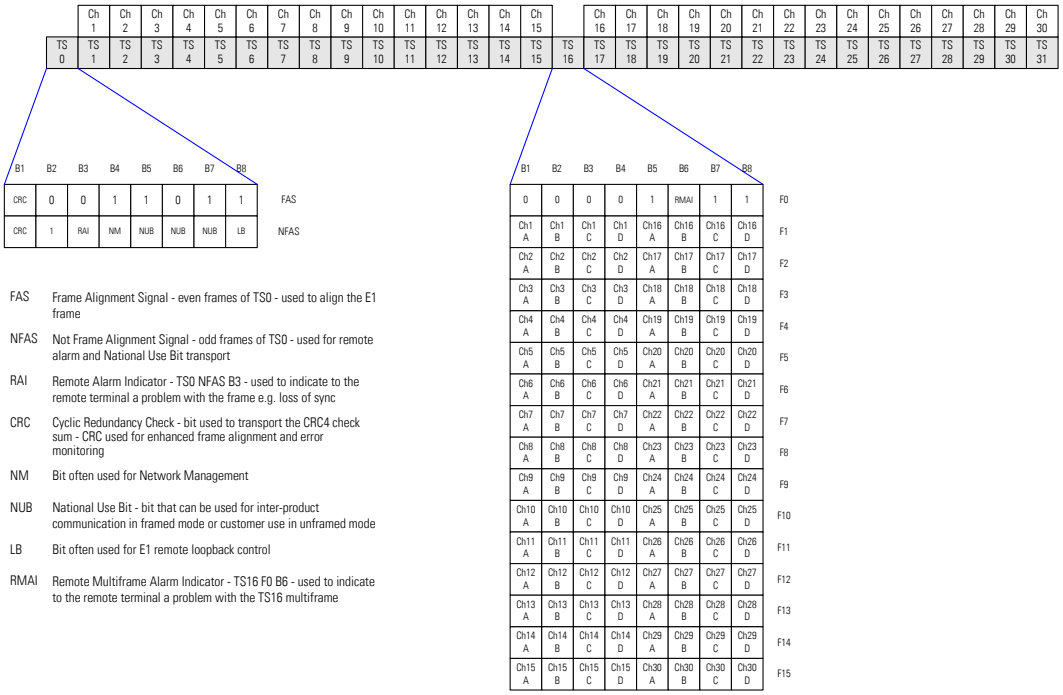
E1 Channel Associated Signalling

E1 Channel Associated Signalling (CAS) uses one timeslot of the G.704 frame (TS16) to transport all the signalling for the 30 PCM channels. It does this by creating a multi-frame structure so that the signalling for each channel gets a share of TS16's bandwidth.

The TS16 multi-frame has 16 frames (F0 for sync and F1-15 for signalling) so each channel gets four bits ABCD, each bit with a bandwidth of 500 bit/s.

The Aprisa XE E1 framing modes of PCM30 and PCM30C use CAS. The TS16 multi-frame is demultiplexed and cross-connected to interface port signalling bits.

G.704 2 Mbit/s E1 Frame



FAS	Frame Alignment Signal - even frames of TS0 - used to align the E1 frame
NFAS	Not Frame Alignment Signal - odd frames of TS0 - used for remote alarm and National Use Bit transport
RAI	Remote Alarm Indicator - TS0 NFAS B3 - used to indicate to the remote terminal a problem with the frame e.g. loss of sync
CRC	Cyclic Redundancy Check - bit used to transport the CRC4 check sum - CRC used for enhanced frame alignment and error monitoring
NM	Bit often used for Network Management
NUB	National Use Bit - bit that can be used for inter-product communication in framed mode or customer use in unframed mode
LB	Bit often used for E1 remote loopback control
RMAI	Remote Multiframe Alarm Indicator - TS16 F0 B6 - used to indicate to the remote terminal a problem with the TS16 multiframe

E1 Common Channel Signalling

E1 Common Channel Signalling (CCS) uses one timeslot of the G.704 frame, usually TS16 but can be any timeslot. The 64 kbit/s bandwidth of the CCS timeslot is used to transport many different types of signalling e.g. ITU No. 7 common channel signalling system

The Aprisa XE framing modes of PCM31 and PCM31C use CCS to transport / pass through a customer entire CAS timeslot or other type of CCS signalling.

Aprisa XE DFXO / DFXS

Aprisa XE Implementation of 2 Wire Loop Interface

The Aprisa XE implementation of 2 wire loop interfaces can be broken down into two major parts;

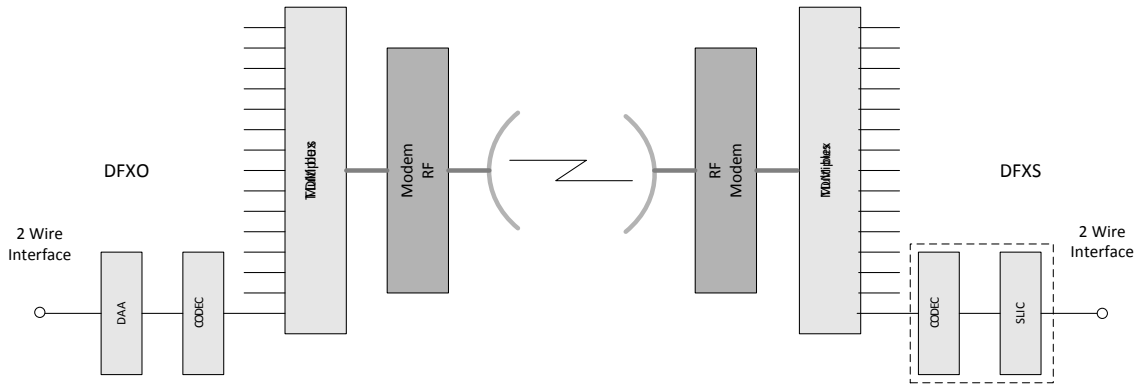
- The 2 wire analogue circuitry that splits the 2 wire bothway voice signals into 4 wire send and 4 wire receive path signals for digitization and multiplexing into the upstream digital signal (send path).
- The 2 wire loop signalling interface circuitry which processes the call setup, call monitoring and call release via DC and AC control signals

SLIC / DAA

The Subscribers Line Interface Chip (SLIC) implements the DFXS 2 wire line interface and signalling conditions. A ProSlic implements a Slic and a Codec in one chip.

The Direct Access Arrangement (DAA) implements the DFXO 2 wire line interface and signalling conditions.

DFXO / DFXS System



2 Wire Analogue

2 Wire Analogue

The following paragraphs define the engineering terms relating to 2 wire analogue circuits:

Codec

The codec (coder decoder) translates between the analogue side of the 2 wire interface to the digital side of the PCM bus.

- The coder digitizes the interface input analogue signal and generates an A law / μ law PCM digital signal, commonly called A-D.
- The decoder takes the received A law / μ law PCM digital signal and reconstructs the analogue signal which is outputted from the interface, commonly called D-A.

Most European countries use the A law companding and North America and Japan use the μ Law companding.

2w / 4w Hybrid

The purpose of the 2w / 4w hybrid is to split the bothway analogue signals on the 2 wire path into separate send and receive 4 wire paths for transmission over the separate send and receive transmission paths.

An ideal hybrid would pass the 2 wire send signal to the 4 wire send and the 4 wire receive signal to the 2 wire receive both without loss. It would also have an infinite loss across the hybrid from the 4 wire receive to the 4 wire send (trans-hybrid).

Practically, the hybrid operation is far from ideal and very dependent on its surrounding impedances. A trans-hybrid loss figure of better than 30 dB between 300 – 3400 Hz is a ‘good’ result.

A 2w / 4w hybrid provides the optimum trans-hybrid loss when its hybrid balance impedance (Zb) is matched to the impedance connected to the 2 wire interface port.

Early derived systems used transformer hybrids but modern codecs implement the hybrid using signal cancellation techniques.

Line Termination Impedance

The line termination impedance (Zt) is the impedance seen looking into the 2 wire interface. It is not the hybrid balance impedance.

Modern codecs synthesize the line termination impedance.

Note: Changing the Aprisa XE DFXO / DFXS line impedance setting changes both the line termination impedance and the hybrid balance impedance to the same value.

Hybrid Balance Impedance

The hybrid balance impedance (Zb) is the impedance network on the opposite side of the hybrid from the DFXO / DFXS line interface.

The purpose of this network is to balance the hybrid to the impedance presented to the DFXO / DFXS line interface.

The trans-hybrid loss is optimized when this impedance matches the impedance of the external 2 wire line.

Modern codecs synthesize the hybrid balance impedance.

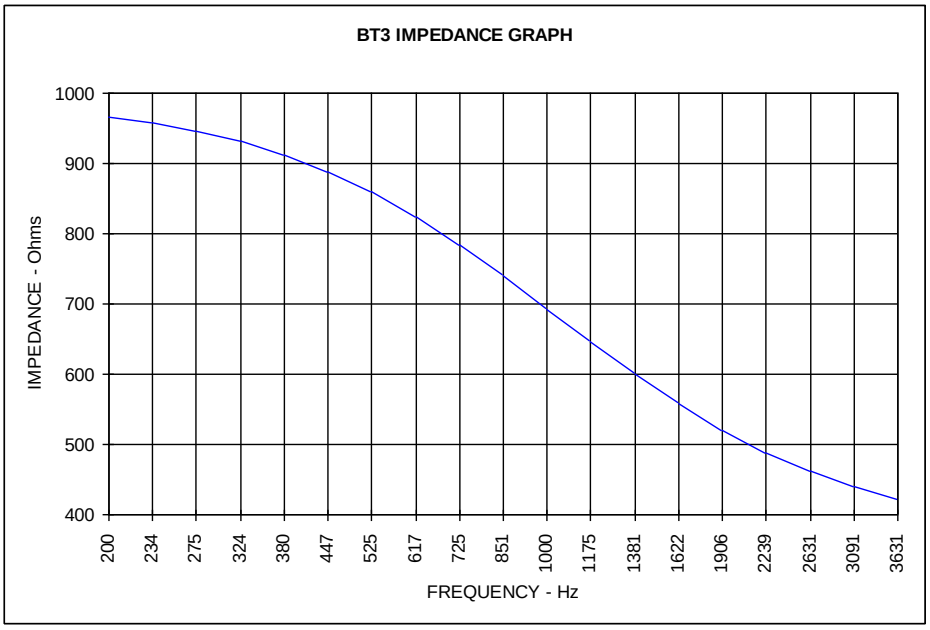
Note: Changing the Aprisa XE DFXO / DFXS line impedance setting changes both the line termination impedance and the hybrid balance impedance to the same value.

Complex Impedance

Traditionally, transmission products where interconnected with a termination impedance of 600 Ω. This maintains a constant impedance (600 Ω) across the frequency band of interest.

However, cable pairs do not exhibit a constant impedance across the voice frequency band (300 to 3400 Hz), but rather produce a variable or complex impedance depending on the frequency.

Complex impedance networks were produced by modelling the characteristic impedance of typical cable pairs. The construction of copper cable varies between manufacturers / countries, so various complex networks came to be e.g. BT3 (UK), TN12 (Australia), TBR21 (Europe):



Short interconnecting copper pairs (< 100 meters) between 2 wire interfaces have little effect on the circuit impedance. The interface line termination impedances are the dominant factors, so the interface line impedance settings can be a non-complex value e.g. 600 Ω or a complex line impedance (e.g. TBR21, TN12, BT3).

As the length of the interconnecting copper pair is increased, the impedance of the copper line has a greater effect on the circuit impedance. For this reason, a complex line termination impedance that matches the characteristic impedance of the copper pair should be used (e.g. TBR21, TN12, and BT3).

Trans-hybrid Loss

Trans-hybrid Loss is a measure in dB of how much analogue signal received from the remote terminal is passed across the hybrid and sent to the remote terminal. Terminal Balance Return Loss (TBRL) is a measure of the trans-hybrid loss as seen via the level adjustment circuitry.

The trans-hybrid loss is maximized when the hybrid balance impedance matches the impedance presented to the DFXO / DFXS line interface. An optimized hybrid minimizes circuit echo.

The specification for the Aprisa XE DFXO / DFXS interfaces is:

better than 13 dB 300 Hz to 3400 Hz

better than 17 dB 500 Hz to 2500 Hz

(with matched external line and hybrid balance impedance)

Return Loss

Return Loss is a measure in dB of the degree in impedance matching between the desired impedance and the actual impedance, for example:

Desired Impedance	Actual Impedance	Return Loss	Impedance Error
600 Ω	612 Ω	40 dB	2%
600 Ω	639 Ω	30 dB	7%
600 Ω	730 Ω	20 dB	22%
600 Ω	1150 Ω	10 dB	92%

The specification for the Aprisa XE DFXO / DFXS interfaces is:

better than 12 dB 300 Hz to 600 Hz

better than 15 dB 600 Hz to 3400 Hz

Common Mode Rejection Ratio

Common mode rejection ratio (CMRR) is a measure in dB of the ability of the interface to reject common mode signals with respect to ground.

On a balanced cable pair, crosstalk caused by interfering signals from other cable pairs, appear as common mode longitudinal or transverse signals at the interface. An ideal balanced interface port would cancel out these unwanted common mode signals and pass only the wanted differential signal.

The specification for the Aprisa XE DFXO / DFXS interfaces is:

better than 40 dB 50 Hz to 3800 Hz

better than 46 dB 600 Hz to 3400 Hz

Circuit Levels

The circuit levels and the trans-hybrid loss of both ends of the circuit, determine the stability of the circuit. If the circuit levels are too high and the trans-hybrid loss figures achieved are too low, the circuit can have a positive loop gain and will recirculate (sometimes called singing).

Typically, a 2 wire voice circuit is engineered to have a 2-3 dB loss in both directions of transmission to maintain circuit stability under most line conditions.

The 8 bit digital word for each analogue sample encoded (A law), has a maximum of 255 quantizing code steps, + 127 for positive signals, -127 for negative signals and 0.

A nominal level of 0 dBm generates a peak code of ± 118 which allows up to +3.14 dBm0 of headroom before the maximum step of 127 is obtained. Any level greater than +3.14 dBm0 will be distorted (clipped) which will cause severe problems with analogue data transmission.

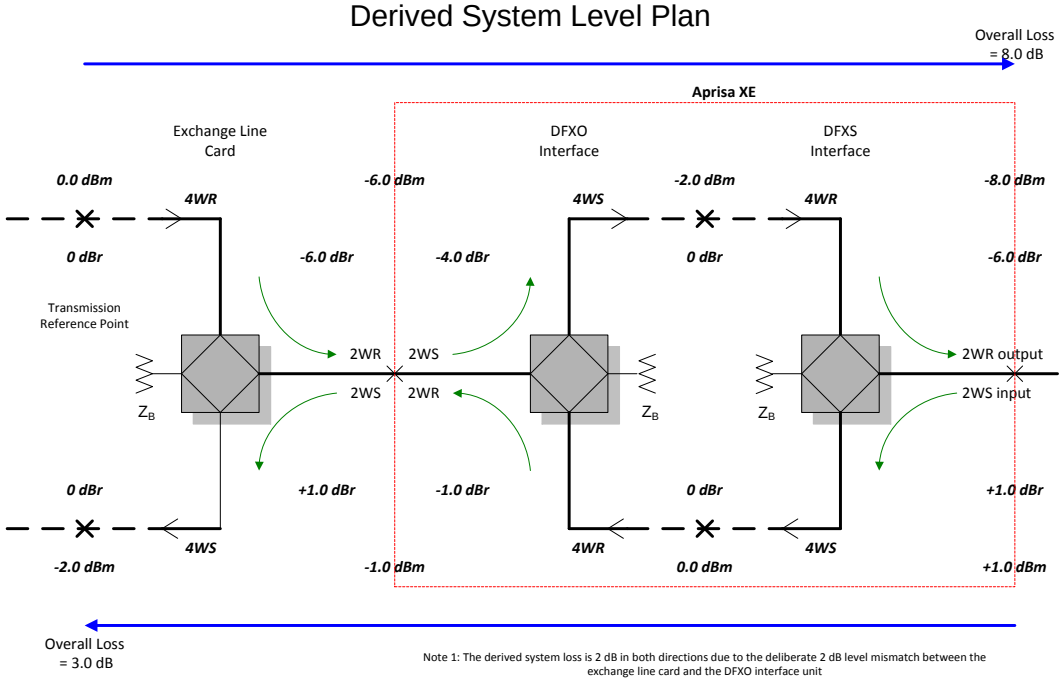
It is therefore important that analogue signals presented from the DFXO / DFXS line interface be normalized to fit within the ± 127 quantizing steps. This is done by adjusting the circuit levels relative to the 0 dBm (± 118 peak code) for example:

- If a nominal input level of +1 dBm is applied to the DFXS line interface, the DFXS Input Level must be set to +1.0 dBr. This will effectively attenuate the sent signal by 1 dB to produce 0 dBm at the coder.
- If a nominal output level of -6 dBm is required from the DFXS line interface, the DFXS Output Level must be set to -6.0 dBr. This will effectively attenuate the output of the decoder 0 dBm signal by 6 dB.

The following shows a typical Derived System Level Plan.

The input and output dBr levels shown are the default Aprisa XE DFXO / DFXS levels when the product leaves the factory. This enables circuits provisioned with the Aprisa XE to operate correctly without changing the levels.

Derived System Level Plan



Note 1: The derived system loss is 2 dB in both directions due to the deliberate 2 dB level mismatch between the exchange line card and the DFXO interface unit

Echo Canceller

If the circuit quality achieved is poor, any signal sent into the 2 wire port will be returned at a level determined by the circuit loop gain and delayed by the circuit round trip delay. The measurement of this echo is referred to as 'echo return loss'.

The longer the round trip delay, the worse the effect of echo becomes on your conversation.

The DFXO Echo Canceller provides up to 64 ms of echo cancellation of echo appearing at the input of the DFXO. This feature is only available on Rev D (and later) DFXO cards.

Telephone Loudness Rating

Telephone Loudness rating (often called receive objective loudness rating), is the ratio in dB of the voltage entering a telephone to the sound pressure produced by the telephone's receiver.

Feed Bridge

The Feed Bridge allows the DC signalling / DC line feed to be superimposed on the 2 wire line without affecting the AC impedance of the circuit.

2 Wire Loop Signalling

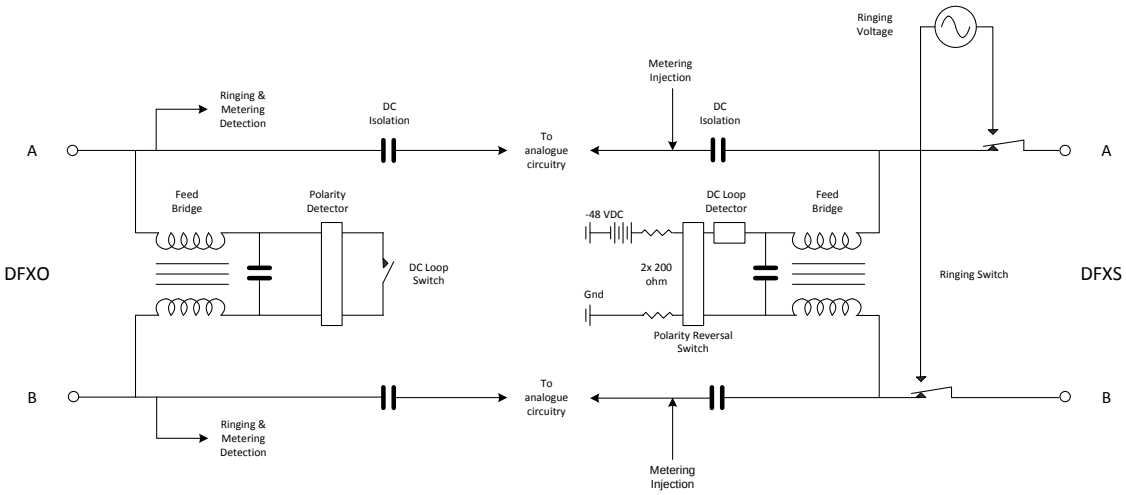
DFXO / DFXS Interface Representation

DFXO / DFXS Interfaces

The following diagram is a representation of the 2 wire loop signalling circuitry used to build the DFXO and DFXS interfaces.

Before the advent of SLICs and DAA chips, this was actually how loop interfaces were built.

DFXO / DFXS Signalling



Aprisa XE Signalling Modes

The Aprisa XE currently has three types of signalling modes that can apply to DFXO or DFXS cross connections.

Multiplexed mode

Multiplexers the four ABCD bits from the interface into a single 8 kbit/s channel.

This is the most efficient as it only requires 8 kbit/s of radio link capacity but cannot be used for interworking between framed E1 / T1 and voice interfaces.

Non-multiplexed mode

Transports each of the four ABCD bits in separate 8 kbit/s channels.

This is inefficient as it requires 8 kbit/s of radio link capacity for each signalling bit but allows interworking between framed E1 / T1 and voice interfaces.

4 wire compatible mode

This signalling is a 1 bit protocol (CAS A bit only) used to interwork between a DFXS interface and a Q4EM interface or between a DFXS interface and a QJET to provide E1 CAS to DFXS circuits.

DFXO Signalling Conditions

DFXO Signalling

The following DFXO signalling conditions apply to a multiplexed or non-multiplexed cross connection between a DFXO and DFXS interface.

This signalling uses a 4RF proprietary implementation using all four CAS bits ABCD available to each timeslot.

DFXO Idle

When the circuit is idle, the DFXO monitors the -48 VDC line voltage output from the exchange line card and is able to detect a DC polarity reversal or AC ringing signal from the exchange.

The DFXO is ready to be signalled by the CAS bit to loop the exchange line (DFXO DC Loop output).

The Aprisa XE uses the CAS A bit = 1 in the DFXS to DFXO direction to signal the DC loop make output condition.

The Aprisa XE DFXO will output a 'fxoUnplug' alarm if it does not detect the exchange line voltage (e.g. if the exchange line is disconnected).

DFXO Ringing Detection

Ringing is a high voltage AC signal (typically 40-75 V rms 25 Hz source) sent from the exchange line card to 'ring' the telephone.

The DFXO detects the cadence of the AC ringing bursts from the exchange line card (ring on / ring off periods) and signals the DFXS to output the same ringing cadence with the CAS B bit in the DFXO to DFXS direction. CAS B = 0 for ringing on and CAS B = 1 for ringing off.

The Aprisa XE specification for DFXO ringing detection is:

> The DFXO has an adjustable Ringing detection threshold of 16 Vrms, 26 Vrms or 49 Vrms over a frequency range of 15 to 50 Hz sine wave. It also has a selectable ringing input impedance of >1 MΩ or 12 kΩ.

DFXO DC Loop Output

The DFXO provides a low resistance DC path which 'loops' the exchange line.

The Aprisa XE uses the CAS A bit = 0 in the DFXS to DFXO direction to signal the DC loop for either Ring trip (outgoing call) or Off Hook (incoming call).

The DFXO provides a current limit option (60mA) but most exchanges also provide a current limit on the line feed. As a general rule, only one interface should current limit so if the exchange interface current limits, the DFXO interface should be set to current limit off.

The DFXO also provides a current overload limit of 160mA and an alarm 'fxoCurrentOvld' if activated.

DFXO Switch Hook Flash

Switch Hook Flash (SHF) is used to activate smartphone services e.g. call waiting - switching between callers.

The DFXS detects the Switch Hook Flash as a loop break pulse of between 100-1000 ms and signals the DFXO to output the SHF signal to the exchange.

DFXO Dialling

Dialling is used to convey the called customer number required from the calling customer to the exchange.

There are two types of dialling are used to signal the exchange;

- DTMF (or tone dialling) is an AC signal comprising 2 out of 5 tones representing the 12 keys on the keypad. The phone sends these tones to the DFXS which transports them back to the DFXO and exchange via the analogue speech path.
- Decadic (or pulse dialling) is multiple DC loop dis-connect pulses typically at 10 PPS (pulses per second). These loop break pulses are detected by the DFXS which signals the DFXO with the CAS A bit in the DFXS to DFXO direction which replicates the loop break pulses to the exchange. CAS A bit = 1 for loop break and CAS A bit = 0 for loop make.

The Aprisa XE specification for decadic dialling is:

> The Aprisa XE provides transparent decadic signalling over a range of 7 - 14 PPS with break period limits of 60 - 73 % (with a DFXS loop current > 23 mA).

DFXO DC Polarity Reversal Detection

If the DFXO detects a DC polarity reversal from the exchange line card, it signals the DFXS with the CAS D bit DFXO to DFXS direction and the DFXS outputs a DC polarity reversal to the customer.

Polarity reversal occurs for two possible situations;

- The Polarity reversal condition is used during an outgoing call to signal the pending arrival of ringing, commonly called a fast guard reversal (guards against PBX systems picking the same trunk for an incoming call).
- The Polarity reversal condition is used during an incoming call to indicate that the called party has answered the call. This signal is usually used for call supervision / billing in PBX systems etc but not usually used for ordinary telephones.

DFXO Metering Detection

Pulse Metering (also known as billing tones) are periodic bursts of 12 or 16 kHz AC tones sent from the exchange to the subscriber to indicate the rate of charge e.g. an expensive toll call may be signalled every second but a cheap call maybe only every 30 seconds.

The DFXO detects the metering bursts from the exchange line card and signals the DFXS with the CAS C bit in the DFXO to DFXS direction and the DFXS replicates the metering bursts to the customer. CAS C bit = 0 for metering on and CAS C bit = 1 for metering off.

Metering is typically used by payphones, hotels and some businesses to calculate the charge to the customer.

The Aprisa XE specification for metering detection is:

> The DFXO has an adjustable metering level sensitivity of -17dBm to -40 dBm in 1dB steps into 200 ohms (60 mV rms to 5 mV rms into 200 ohms). The maximum level of metering signal the DFXO can tolerate without voice band interference is 0.8 Vrms into 200 ohms.

DFXO Caller ID

Caller ID information is transported in the speech path during the first long ringing silent period (> 800ms) as a burst of 1200 baud FSK data.

The DFXO is transparent in the speech path to the analogue Caller ID information.

Caller ID sent over an analogue path is referred to ACLIP (Analogue Calling Line Identification Presentation).

DFXS Signalling Conditions

DFXS Signalling

The following DFXS signalling conditions apply to a multiplexed or non-multiplexed cross connection between a DFXO and DFXS interface.

This signalling uses a 4RF proprietary implementation using all four CAS bits ABCD available to each timeslot.

DFXS Idle

When the circuit is idle, the DFXS outputs a DC 'line feed'. This is a -48 VDC voltage with a source resistance of 320 Ω and current limited to between 35 mA.

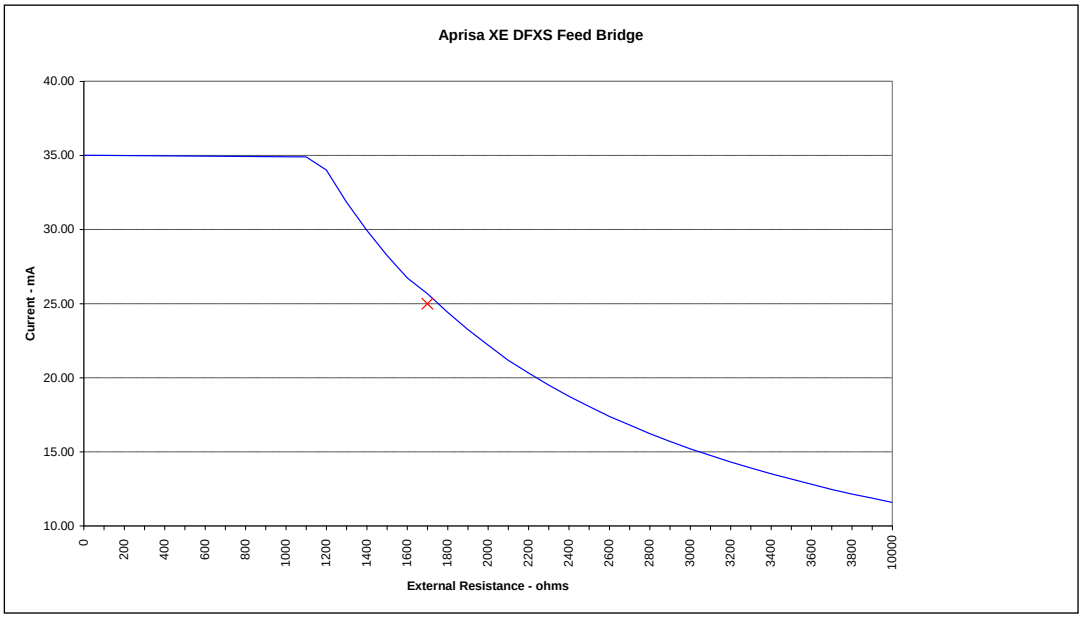
This DC voltage line feed effectively powers the telephone and allows for detection of an off-hook and decadic signalling.

The feed bridge voltage / current limit point, the source resistance and the loop resistance of the telephone all determine the Copper Loop Operating range of the interface.

The Aprisa XE specification for line feed is:

The Aprisa XE DFXS uses a -48 VDC 160 + 160 Ω voltage source current limited to 35mA.

With a typical telephone DC loop resistance of 450 Ω, a minimum loop current of 25mA and 0.4mm copper at a loop resistance of 273 Ω per km, the DFXS has a Copper Loop Operating range of 4 km.



DFXS Ringing Output

Ringing is a high voltage AC signal (typically 40-75 Vrms 25 Hz source) sent from the exchange to 'ring' the phone. The ringing AC voltage usually has a DC offset voltage to enable ring trip to occur with a DC loop during the ring on cycle.

The DFXO detects the cadence of the AC ringing bursts from the exchange line card (ring on / ring off periods) and signals the DFXS to output the same ringing cadence with the CAS B bit in the DFXO to DFXS direction. CAS B = 0 for ringing on and CAS B = 1 for ringing off.

The ringing output power required from the DFXS is determined by the ringing voltage, the line length and the number of REN required to ring into.

The Aprisa XE specification for DFXS ringing output is:

> The ringing output is a composite balanced AC ringing voltage with a differential DC offset voltage.
>
> 60 Vrms + 0 VDC
>
> 55 Vrms + 10 VDC
>
> 50 Vrms + 18 VDC
>
> 45 Vrms + 22 VDC
>
> 40 Vrms + 24 VDC

DFXS Ringing Load (REN)

The REN (Ringer Equivalent Network) value is important in determining how many phones can be rung simultaneously on a single line by the system delivering the ringing.

The original REN represented the effective impedance of an old style telephone bell circuit which used electro-mechanical bells for ringing.

If there were a large number of phones connected across the one line, the combined ringing load was so great that the ringing voltage was not sufficient to ring the bells and none of the phones would ring. This was a common problem with old style phones.

Modern phones use electronic ringers which use much less power and hence have significantly higher impedance to ringing than the old bell phones. These phones often have 1/10 REN or lower which means that many more phones can be rung on the same line from the same system.

Unfortunately, each country has their own definition of REN based on their legacy phones. Some of our customer REN values are:

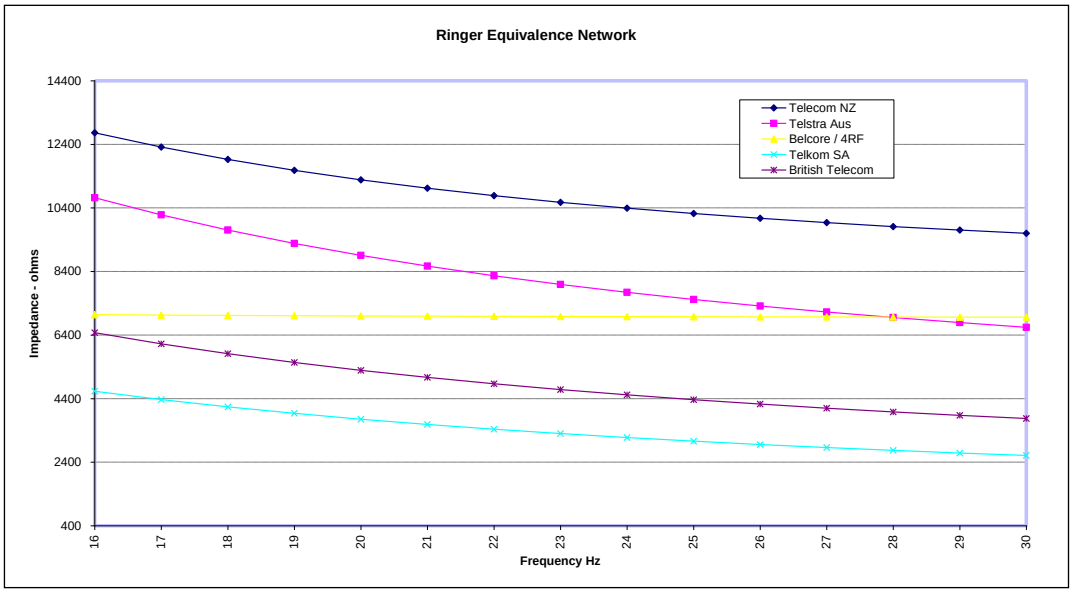
Belcore / 4RF	6930 Ω in series with 8 µF
British Telecom	1800 Ω in series with 1.6 µF
Telecom NZ	8000 Ω in series with 1 µF
Telkom SA	1000 Ω in series with 2.2 µF
Telstra Aus	4000 Ω in series with 1 µF

Note:

4RF has standardized on the Belcore definition of REN which is 6930 Ω in series with 8 µF which has an impedance of 6976 Ω at 25 Hz.

The Aprisa XE specification for DFXS ringing output power is:

60 Vrms source into a load of 2 REN
45 Vrms source into a load of 3 REN
(1 REN ≈ 6930 Ω in series with 8 µF)



DFXS Ring Trip

Ring trip occurs when the customer picks up the handset when the phone is ringing.

The DFXS stops the ringing output and signals the DFXO with the CAS A bit in the DFXS to DFXO direction. CAS A = 0 for ring trip. This replicates the ring trip towards the exchange. i.e. similar to off-hook.

The Aprisa XE specification for ring trip is:

Ring trip will occur in < 150 ms following DC loop of > 20 mA

Ring trip will not occur if the DFXS outputs ringing into a load of 500 Ω in series with 4.4 µF or less

DFXS DC Polarity Reversal Output

The DFXS is signalled to output a DC polarity reversal to the customer by a CAS D bit DFXO to DFXS direction. CAS D bit = 0 for polarity reversal.

Polarity reversal occurs for two possible situations;

- The Polarity reversal condition is used during an outgoing call to signal the pending arrival of ringing, commonly called a fast guard reversal (guards against PBX systems picking the same trunk for an incoming call).
- The Polarity reversal condition is used during an incoming call to indicate that the called party has answered the call. This signal is usually used for call supervision / billing in PBX systems etc but not usually used for ordinary telephones.

DFXS Off Hook

When a customer picks up the handset, the telephone provides a DC loop across the cable pair. DC loop current drawn from the DFXS is detected as an off-hook.

The DFXS signals the DFXO with the CAS A bit = 0 in the DFXS to DFXO direction which replicates the off hook towards the exchange line card.

DFXS On Hook

When a customer replaces the handset on the telephone, the phone breaks the DC loop across the cable pair. The cessation of DC loop current drawn from the DFXS is detected as an on-hook (or decadic loop break).

The DFXS signals the DFXO with the CAS A bit = 1 in the DFXS to DFXO direction which replicates the on hook towards the exchange line card.

DFXS Switch Hook Flash

Switch Hook Flash (SHF) is used to activate smartphone services e.g. call waiting - switching between callers.

The DFXS detects the Switch Hook Flash as a loop break pulse of between 100-1000 ms and signals the DFXO to output the SHF signal to the exchange.

DFXS Dialling

Dialling is used to convey the called customer number required from the calling customer to the exchange.

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- Decadic (or pulse dialling) is multiple DC loop dis-connect pulses typically at 10 PPS (pulses per second). These loop break pulses are detected by the DFXS which signals the DFXO with the CAS A bit in the DFXS to DFXO direction which replicates the loop break pulses to the exchange. CAS A bit = 1 for loop break and CAS A bit = 0 for loop make.

Note:

Some countries (e.g. New Zealand) standardized on the UK format called 'reverse decadic' where the number of pulses sent is 10 minus the number dialled e.g. dialling an 8, sends 2 decadic pulses.

The Aprisa XE specification for pulse dialling is:

> Transparent decadic signalling at 7 - 14 PPS with break period limits of 60 - 73 % (with loop current > 23 mA).

DFXS Metering Output

Pulse Metering (also known as billing tones) are periodic bursts of 12 or 16 kHz AC tones sent from the exchange to the subscriber to indicate the rate of charge e.g. an expensive toll call may be signalled every second but a cheap call maybe only every 30 seconds.

The DFXO detects the metering bursts from the exchange line card and signals the DFXS with the CAS C bit in the DFXO to DFXS direction and the DFXS replicates the metering bursts to the customer. CAS C bit = 0 for metering on and CAS C bit = 1 for metering off.

Metering is typically used by payphones, hotels and some businesses to calculate the charge to the customer.

The Aprisa XE specification for DFXS metering output level is:

Line Impedance	Max output into 200 Ω
TN12, TN12 and TBR21	400 mV rms
BT3	300 mV rms
600 Ω and 900 Ω.	200 mV rms

DFXS Caller ID

Caller ID information is transported in the speech path during the first long ringing silent period (> 800ms) as a burst of 1200 baud FSK data.

The DFXS receives the analogue Caller ID information in the speech path and outputs the signal to the called party in the first long ringing silent period.

Caller ID sent over an analogue path is referred to ACLIP (Analogue Calling Line Identification Presentation).

Telecom Network Analogue Performance

Network Performance

The analogue performance of a Telecom network is very dependent on the number of '2 wire interconnect points' in the overall end to end circuit (telephone to telephone).

A '2 wire interconnect point' occurs when a DFXS interface is connected to a DFXO interface or an DFXS interface is connected to a telephone.

Each 2 wire interconnect point adds an additional D-A and A-D conversion and a 4 wire to 2 wire / 2 wire to 4 wire conversion.

The end to end network performance is degraded for each additional 2 wire interconnect point which results in lower circuit levels and an increased possibility of circuit echo.

For example:

1. If an exchange 2 wire line card (DFXS) is extended to a remote site with a network product like the Aprisa XE, the interconnect between the exchange line card and the DFXO has added an additional 2 wire interconnect point. If a call is made between two phones at the remote site, the call has traversed four 2 wire interconnect points.

2. If an exchange 2 wire line card (DFXS) is extended to a remote site with a two cascaded network products, two additional 2 wire interconnect points have been added. If a call is made between two phones at the remote site, the call has traversed six 2 wire interconnect points. Speech levels would be low and analogue data service would almost be unusable.

To achieve the best overall network performance, the number 2 wire interconnect points should be minimized.

Network System Interconnect

A digital interface is the best method of interconnect between network systems as it does not degrade the end to end circuit performance.

The next best method of interconnect between network systems is with 4 wire E&M. This method still has an additional D-A and A-D conversion but no 4 wire to 2 wire / 2 wire to 4 wire conversion.

The ideal network topology only has one 2 wire interconnect point at each end of the entire network i.e. when the DFXS interface connects to the telephone with all intermediate interconnects at digital.

2 Wire Interconnect Point

The circuit quality achieved with a 2 wire interconnect point is very dependent on the setup of the external interfaces connected to it

Rules to improve circuit quality:

- The impedance of the line must match the interface hybrid balance impedance (Zb).

  The impedance of the line is usually a combination of the copper cable pair and the line termination impedance of the product connected to the line.
- The line termination impedances of both product interfaces must match.

  e.g. the Zt of the exchange line card and the DFXO must be the same.
- The circuit levels of the exchange, interface cards and the telephone can all affect the circuit quality.

  If echo is present, high circuit levels can only make the echo more apparent.
- The common mode balance of all the 2 wire interfaces must be sufficient to reject interfering signals on the cable pairs.

When the impedance matches are improved, the trans-hybrid loss is improved therefore the possibility of echo is reduced.

Common 2 Wire Interconnect Problem

One of the most common problems with interconnecting 2 wire loop interfaces between products is cause by impedance mismatch with the following scenario:

- Aprisa XE link providing DFXO / DFXS circuits from telephone to the exchange
- DFXO Line Impedance set to TBR21
- Exchange line termination and hybrid balance impedance set to 600 Ω

The result of this mismatch causes multiple circuit problems:

1. The circuit levels will be incorrect, as the DFXO source impedance is complex TBR21 and the line card line termination impedance is 600 Ω.
2. The DFXO hybrid will be unbalanced because it has 600 Ω on one side and TBR21 on the other. This will allow more received signal to be circulated back to the originator (telephone) as echo (red lines).
3. The exchange line card hybrid will be unbalanced because it also has 600 Ω on one side and TBR21 on the other. This will produce echo for the other caller.